What is claimed is:

[Claim 1] 1. A method for fabricating a flash memory device, comprising:

forming a tunneling oxide layer over a substrate;
forming a charge storage layer over the tunneling oxide layer; and
performing a thermal oxidation process so that a portion of the charge storage layer is oxidized to form an inter-gate dielectric material layer, while other portion of the charge storage layer not being oxidized is converted into a plurality of nanocrystals, wherein the nanocrystals form a floating gate.

[Claim 2] 2. The method of claim 1, wherein the step of forming the charge storage layer comprises forming a Si_XGe_{1-X} layer or forming a metal silicide layer.

[Claim 3] 3. The method of claim 2, wherein the charge storage layer comprising Si_XGe_{1-X} is formed by performing a low pressure chemical vapor deposition (LPCVD) process with a reactive gas of SiH_4 or GeH_4, under an operating pressure between 1 and 1000 mTorrs, and an operating temperature is between 600 and 800 degrees centigrade.

[Claim 4] 4. The method of claim 2, wherein the metal silicide layer comprises tungsten silicide, titanium silicide, cobalt silicide or nickel silicide.

[Claim 5] 5. The method of claim 4, wherein the charge storage layer comprises W_YSi_Z, and the value of Y is between 0.5 and 5, and the value of Z is between 1 and 3.

[Claim 6] 6. The method of claim 5, wherein the charge storage layer is formed by performing a low pressure chemical vapor deposition (LPCVD) process with a reactive gas of WF_6, SiH_4, Si_2H_6,SiH_2Cl_2, or a composition

thereof, under an operating pressure between 1 and 1000 mTorrs, and an operating temperature between 300 and 800 degrees centigrade.

[Claim 7] 7. The method of claim 1, wherein the thermal oxidation process comprises a rapid thermal oxidation process.

[Claim 8] 8. The method of claim 7, further comprising:

providing gases including oxygen during the rapid thermal oxidation process.

[Claim 9] 9. The method of claim 8, wherein the gases including oxygen comprises O_2, H_2O or NO_x.

[Claim 10] 10. The method of claim 7, wherein a process temperature of the rapid thermal oxidation process is between 850 and 1000 degrees centigrade.

[Claim 11] 11. The method of claim 1, wherein the charge storage layer is formed by performing a low pressure chemical vapor deposition (LPCVD) process.

[Claim 12] 12. The method of claim 1, wherein the thermal oxidation process further comprises:

forming a control gate over the inter-gate dielectric layer, wherein a stacked gate structure includes the tunneling oxide layer, the floating gate, the inter-gate dielectric layer and the control gate; and
forming a source/drain region in the substrate at each side of the stacked gate structure.

[Claim 13] 13. A structure of a flash memory device comprises:

a substrate;

a tunneling oxide layer disposed over the substrate;
a floating gate disposed over the tunneling oxide layer, and the floating gate includes a plurality of nanocrystals; and
an inter-gate dielectric layer covering the nanocrystals and keeping the nanocrystals within the floating gate, wherein the material of the inter-gate dielectric layer is an oxide of the material of the floating gate.

[Claim 14] 14. The structure of claim 13, wherein the material of the floating gate comprises Si_XGe_{1-X} or metal silicide.

[Claim 15] 15. The structure of claim 14, wherein the material of the metal silicide comprises tungsten silicide, titanium silicide, cobalt silicide or nickel silicide.

[Claim 16] 16. The structure of claim 15, wherein the material of the floating gate comprises W_YSi_Z, and the value of Y is between 0.5 and 5, and the value of Z is between 1 and 3.

[Claim 17] 17. The structure of claim 13, further comprising:

a control gate disposed over the inter-gate dielectric layer, wherein a stacked gate structure includes the tunneling oxide layer, the floating gate, the inter-gate dielectric layer and the control gate; and
a source/drain region formed in the substrate at each side of the stacked gate structure.